CH397 Datasheet

V1.5

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Overview

CH397 is a highly integrated, low-power USB NIC chip with built-in QingKe RISC-V processor, high-speed USB controller and transceiver PHY compliant with USB2.1 protocol specification, and Ethernet MAC+PHY compliant with IEEE802.3 protocol specification, supporting 10M/100M network. Standard USB host interface for all kinds of desktop computers, laptops, tablets, game consoles, etc., used to extend the Ethernet interface via USB.

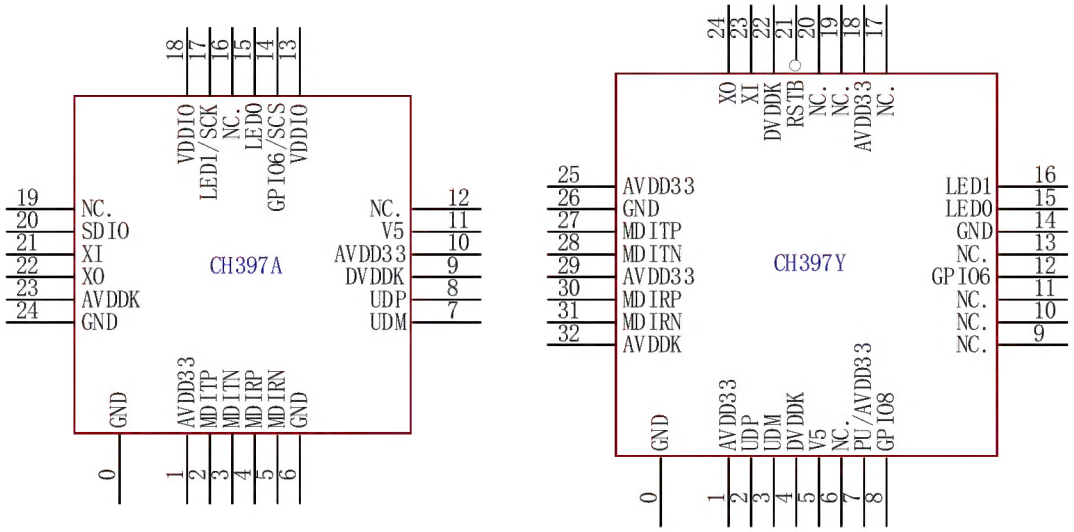
Features

- Single-chip USB2.0/2.1 to 10/100M Fast Ethernet with integrated USB PHY and Ethernet MAC and Ethernet PHY
- Support CDC-ECM protocol, CDC-NCM protocol and RNDIS protocol, no driver installation or optional vendor driver
- Support 10Mbps and 100Mbps rates, IEEE 802.3 10BASE-T/100BASE-TX compatible
- Support 10M/100M Auto-Negotiation
- Built-in TX/RX packet buffering
- Support IPv4/IPv6 packet checksum, support IPv4 TCP/UDP/HEAD and IPv6 TCP/UDP packet checksum generation and inspection
- Support IEEE 802.3x flow control and half-duplex conflict pressure fallback flow control
- Support IEEE 802.3Q VLAN tagging
- Support Sleep mode and low-power Sleep mode, support network low-power configuration, support dynamic power management
- Support remote wake-up via events such as magic packets and network wake-up packets
- Support CAT5 UTP cable, CAT6 UTP cable, support 120 meters transmission distance
- Support Auto-MDIX exchange TX/RX, automatic identification of positive and negative signal lines
- Support LED blinking frequency and duty cycle configuration
- Built-in linear Low-Dropout (LDO) regulator, single power supply
- Built-in 50Ω impedance matching resistor, built-in crystal oscillator capacitor required, peripheral circuitry streamlined
- Processor IP, controller and transceiver IP are all self-developed and tightly integrated, with high efficiency and low-cost, eliminating IP licensing fees
- 6KV enhanced ESD performance, Class 3A
- QFN24, QFN32 and other packages available

Chapter 1 Pin Information

1.1 Pinouts

Figure 1-1 CH397 pinouts



Note: Pin 0# is the EPAD of the QFN package; Smaller QFN packages are also available for volume orders.

1.2 Package

Table 1-1 CH397 package description

Package Form	Body Size	Pin Pitch		Package Description	Order Model
QFN24_4*4	4mm*4mm	0.5mm	19.7mil	Quad Flat No-Lead Package	CH397A
QFN32_4*4	4mm*4mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH397Y

1.3 Pin Definitions

Table 1-2 CH397 pin definitions

Pin No.		Pin name	Type	Function description
397A	397Y			
7	3	UDM	USB	USB2.0 high-speed differential signal cable D-
8	2	UDP	USB	USB2.0 high-speed differential signal cable D+
2	27	MDITP	ETH	Differential transmitter for 10BASE-T/100BASE-TX in MDI mode.
3	28	MDITN	ETH	Differential receiver for 10BASE-T/100BASE-TX in MDIX mode.
4	30	MDIRP	ETH	Differential receiver for 10BASE-T/100BASE-TX in MDI mode.
5	31	MDIRN	ETH	Differential transmitter for 10BASE-T/100BASE-TX in MDIX mode.
21	23	XI	I	Crystal oscillator input, need to connect 25MHz crystal end, or external clock input
22	24	XO	O	Crystal oscillator inverted output, need to connect the other end of 25MHz
11	5	V5	P	5V or 3.3V power input, external 10uF or 4.7uF decoupling capacitor
10	1	AVDD33	P	LDO output and 3.3V analog circuit power input. External 0.1uF+10uF decoupling capacitor, or 1uF decoupling capacitor
13、18	18、	VDDIO	P	Power input for I/O with external 0.1uF or 1uF decoupling capacitor
1	25、29	AVDD33	P	3.3V power input, external 1uF decoupling capacitor
-	7	PU/ AVDD33	P	Pull up to AVDD33 or connect directly to AVDD33
23	32	AVDDK	P	Power supply decoupling terminal of the core analog circuit, external 1uF decoupling capacitor
9	4、22	DVDDK	P	External 0.1uF decoupling capacitor for the power supply decoupling terminal of the core digital circuit
6	14	GND	P	Common ground, necessary connection
24	26	GND	P	Common ground, optional but recommended connection
0	0	GND	P	Common ground (QFN EPAD), necessary connection
15	15	LED0	O	Ethernet port status indicator 0
17	16	LED1	O	Ethernet port status indicator 1
	-	SCK	O	SPI Flash serial clock signal output
14	12	GPIO6	I/O	General-purpose IO interface 6 with built-in pull-up. For chips with lot number penultimate 6 digit 8, this pin defaults to the USB configuration indication ACT after the reset is complete, high before USB configuration, low after USB configuration
	-	SCS	O	SPI Flash chip select signal output, applied during reset and initialization

-	8	GPIO8	I/O	General-purpose I/O interface 8, built-in pull-up
20	-	SDIO	I/O	SPI Flash serial data input/output, connect to SI and SO pins of Flash.
-	21	RSTB	I	External reset input pin, active low, built-in pull-up
12/16/19	6/9/10/11/13/17/19/20	NC		Empty pins or reserved pins, recommended suspension.

Pin types:

(1) I: 3.3V signal input.

(2) O: 3.3V signal output.

(3) P: Power or ground.

(4) USB: USB signal.

(5) ETH: Ethernet signal.

Chapter 2 System Architecture

2.1 System Architecture

Figure 2-1 System block diagram

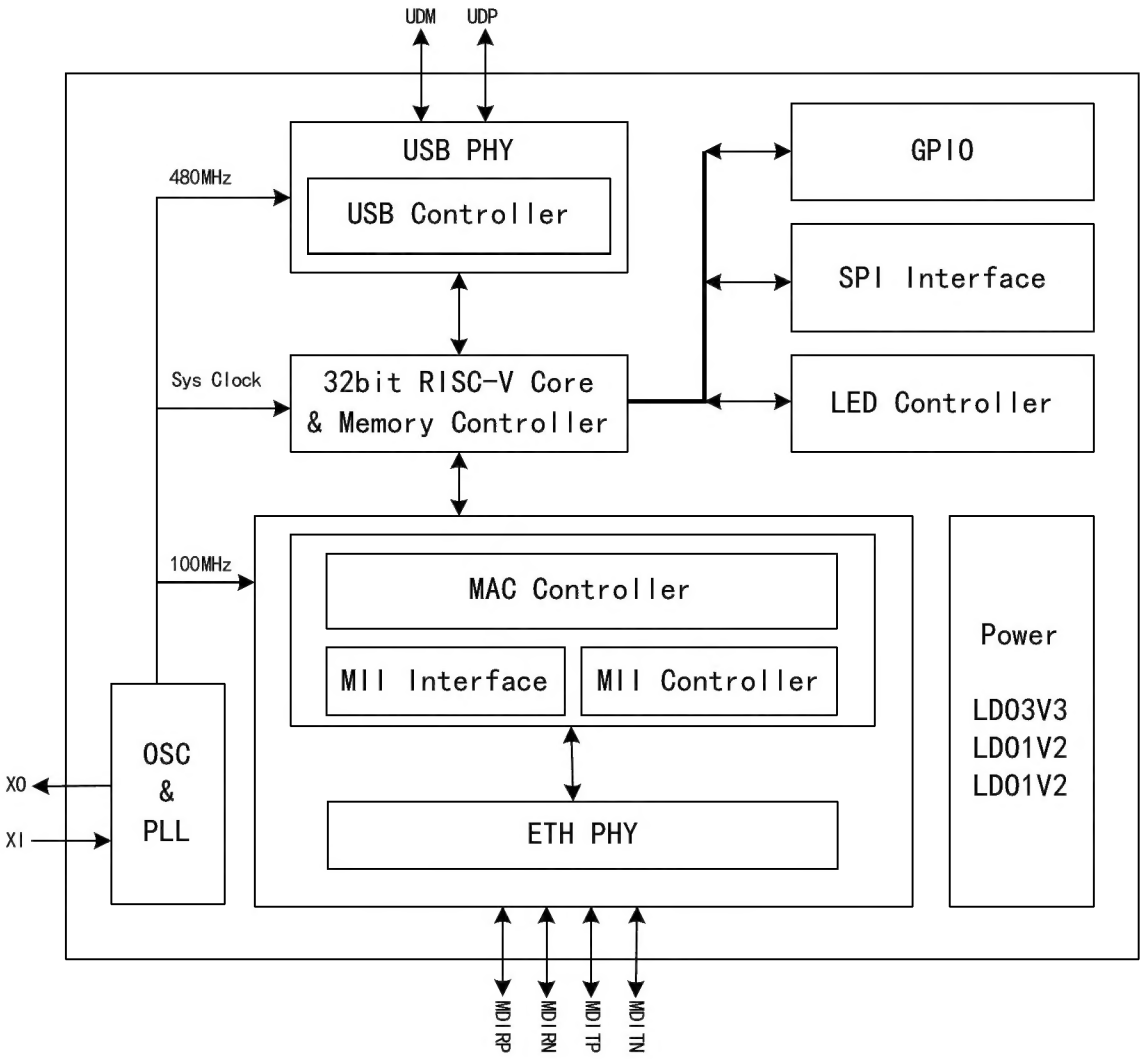


Figure 2-1 is a block diagram of the structure of the USB NIC chip, including USB2.1 controller, USB PHY high-speed transceiver, QingKe RISC-V processor core, Ethernet controller, Ethernet PHY transceiver, etc. All controller IP, transceiver IP and processor core IP are self-developed, with tighter internal connections, high transmission efficiency and low-power consumption. The RISC-V core MCU microcontrollers are used to implement support for multiple protocols, with firmware support for CDC-ECM, CDC-NCM and RNDIS and vendor protocols.

Chapter 3 Basic Functions

3.1 Clock and Reset

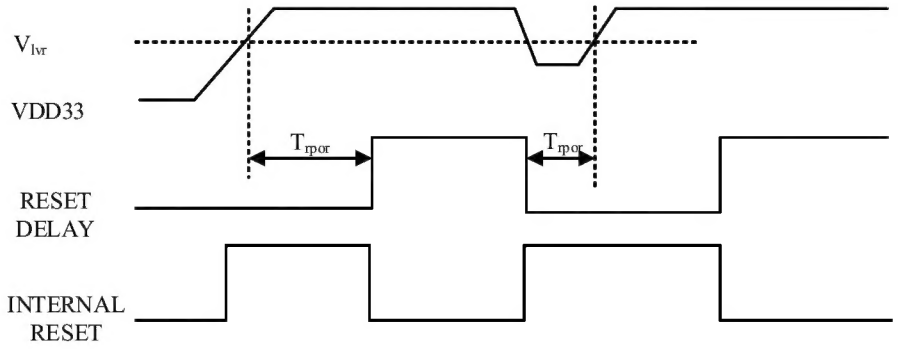
3.1.1 Clock Source

The chip uses an external 25MHz passive crystal with an internal oscillator to provide the clock source, and has built-in load capacitance of 12pF for the two oscillation capacitors required for the external crystal, which is connected to the XI and XO pins to generate the 480MHz clock required for the USB PHY, the 125MHz clock required for the ETH PHY, and the clock for the MCU core via PLL.

3.1.2 Power-on Reset

The chip has an embedded power-on reset module, which generally does not require an external reset signal. When the power supply is powered on, the chip's internal POR power-on reset module generates a power-on reset timing and delays T_{rpor} for about 8~25ms to wait for the power supply to stabilize. During operation, when the power supply voltage falls below V_{lvr}, the chip's internal LVR low-voltage reset module generates a low-voltage reset until the voltage rises again and delays until the power supply stabilizes. Figure 3-1 shows the power-on reset process as well as the low-voltage reset process.

Figure 3-1 Power-on reset



3.1.3 External Reset

The external reset input pin RSTB has a built-in pull-up resistor of about 25 to 50KΩ, so if the chip needs to be reset externally, then the pin can be driven low, and the low-level pulse width of the reset is recommended to be at least 5us.

3.2 USB Interface and Firmware

The integrated USB high-speed device controller and USB-PHY transceiver supports USB2.0/USB2.1 specification at high-speed and full-speed, bus hang, reset, wake-up and resume, and LPM (Link Power Management) functions. Bulk users can customize information such as USB device VID, PID, serial number and vendor string.

The internal firmware supports CDC-ECM mode by default and the custom firmware can support both vendor drivers and CDC-NCM. The firmware will select and enable the appropriate mode based on the user's configuration requirements and commands issued by the PC host.

3.3 10/100M Ethernet

Chip-integrated 10M/100M Fast Ethernet MAC controller and 100GbE transceiver PHY, compatible with IEEE 802.3 10Base-T, 100Base-TX protocol standards. Supports Auto-Negotiation and Auto-MDIX, providing the necessary functions required for transmission over CAT5 network cables and CAT6 network cables. Built-in 50Ω impedance matching resistor and streamlined peripheral circuitry.

The Ethernet controller supports IPv4/IPv6 packet checksum, generation and inspection of IPv4 TCP/UDP/HEAD and IPv6 TCP/UDP packet checksum. Supports IEEE 802.3x-compliant flow control and half-duplex conflict pressure fallback flow control. Support IEEE 802.3Q-compliant VLAN tagging. Support magic packet wake-up, optional network low-power consumption in Sleep mode, with automatic power management function to save power consumption under no load or light load, and support 10Base-T power saving mode.

3.4 LED and GPIO

The CH397 provides 2-channel Ethernet LED control and multiple GPIOs, with some pins time-multiplexed for SPI Flash and other general-purpose function extensions, which can be connected directly. The LED function can be configured by the user, and the relevant configuration options are provided in the User Configuration Tool.

For CH397 chips with lot number penultimate 6 digit 8, the GPIO6 pin is configured by default as the USB configuration status indication ACT.

3.5 SPI Interface

The CH397 provides an SPI interface to an external optional SPI Flash memory chip, which stores custom MAC addresses, MAC filtering configurations, USB vendor IDs, product IDs, USB power configurations, and vendor-defined strings, etc. The SPI clock frequency does not exceed 50MHz.

3.6 SPI FLASH

The CH397 has 2 user configuration loading modes, vendor preset and loading from SPI Flash. When the SPI Flash does not exist or the data in the Flash is invalid, the configuration data preset by the vendor will be used by default. The configuration data includes MAC configuration information including MAC address, USB configuration information, etc. Refer to the relevant manual for details.

3.7 Power Supply

The CH397 supports two power supply modes: external single 5V or single 3.3V. Refer to the following table for the power supply and recommended capacitor values for each pin.

V5	Main AVDD33 with LDO output	Other AVDD33	VDDIO	AVDDK	DVDDK	Description
External supply 5V 3uF～10uF	0.1uF in parallel with 10uF or 4.7uF	1uF	Recommendation: connect AVDD33 0.1～1uF	1uF	0.1～1uF	Single 5V supply, enable the internal LDO, no external LDO step-down, high internal chip
			Optional:			

			down to 2.5V 0.1~1uF			temperature.
External supply 3.3V 0.1～1uF	External supply 3.3V 0.1uF in parallel with 10uF or 4.7uF	External supply 3.3V 1uF	Recommendation: external supply 3.3V 0.1～1uF			Single 3.3V supply, low chip temperature, good for reliability
			Optional: external supply 2.5V 0.1～1uF			

Chapter 4 Parameters

4.1 Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Name	Parameter Description		Min.	Max.	Unit
TA	Ambient operating temperature	V5 and AVDD33 external supply 3.3V	-40	85	℃
		4.6V < V5 voltage <= 5.0V	-40	85	℃
		5.0V < V5 voltage <= 5.3V	-40	70	℃
TS	Ambient temperature during storage		-55	150	℃
V5	LDO input supply voltage (V5 pin to power, GND pin to ground)		-0.4	5.5	V
VDDIO	I/O supply voltage (VDDIO pin to power, GND pin to ground)		-0.4	4.0	V
AVDD33	Analog supply voltage (AVDD33 pin to power, GND pin to ground)		-0.4	4.0	V
AVDDK	Power supply decoupling terminal of the core analog circuit		-0.4	1.5	V
DVDDK	Power supply decoupling terminal of the core digital circuit		-0.4	1.5	V
VBUS	Voltage on USB signal pin		-0.4	AVDD33+0.4	V
VETH	Voltage on ETH signal pin		-0.4	AVDD33+0.4	V
VGPIO	Voltage on other input or output pins (excluding XI and XO)		-0.4	VDDIO+0.4	V
VESD	External HBM mannequin ESD tolerant voltage on I/O pins		5K	7K	V

4.2 Electrical Parameters (Test conditions: TA=25℃, V5=5V or V5=AVDD33=3.3V, VDDIO=AVDD33)

Name	Parameter Description		Min.	Typ.	Max.	Unit
V5	For chips with lot number penultimate 6 digit 0, LDO input supply voltage @ V5	LDO enabled	4.6	5.0	5.25	V
	For chips with lot number penultimate 6 digit 8, LDO input supply voltage @ V5	LDO enabled	4.0	5.0	5.25	
	External 3.3V supply @ V5	No internal LDO required	3.2	3.3	3.45	
AVDD33	Internal LDO output voltage	LDO enabled	3.2	3.3	3.45	V

	@ AVDD33					
	External 3.3V supply @ AVDD33	No internal LDO required	3.2	3.3	3.45	
VDDIO	External supply of 3.3V (or shorted to AVDD33) or 2.5V		2.3	3.3	3.5	V
ILDO	Internal AVDD33 power regulator LDO external load capability				20	mA
ICC	Operating current	100Base-T Heavy Load		75		mA
		100Base-T Idle Load		70		mA
		10Base-T Heavy Load @ Traditional Mode		80		mA
		10Base-T Heavy Load @ Power Saving Mode		65		mA
		10Base-T Idle Load @ Power Saving mode		42		mA
		Ethernet connection disconnected		52		mA
		USB connection disconnected		17		mA
ISLP1	L1 sleep power current with fast wake support			8	12	mA
ISLP0	L0 deep sleep supply current (without 1.5K Ω pull-up) Or: own sleep power current (not connected to USB host)			0.2	0.4	mA
VIL	Low level input voltage	VDDIO=3.3V	0		0.8	V
		VDDIO=2.5V	0		0.7	V
VIH	High level input voltage	VDDIO=3.3V	1.9		VDDIO	V
		VDDIO=2.5V	1.5		VDDIO	V
VOL	Low level output voltage	Input 5mA current @VDDIO=3.3V		0.4	0.6	V
		Input 3mA current @VDDIO=2.5V		0.4	0.6	V
VOH	High level output voltage	Output 5mA current @VDDIO=3.3V	VDDIO-0.6	VDDIO-0.4		V
		Output 3mA current @VDDIO=2.5V	VDDIO-0.6	VDDIO-0.4		V
IPU	RSTB and GPIO pull-up current		20	50	80	uA
Vlvr	Voltage threshold for power supply low-voltage reset		2.6	2.8	3.1	V

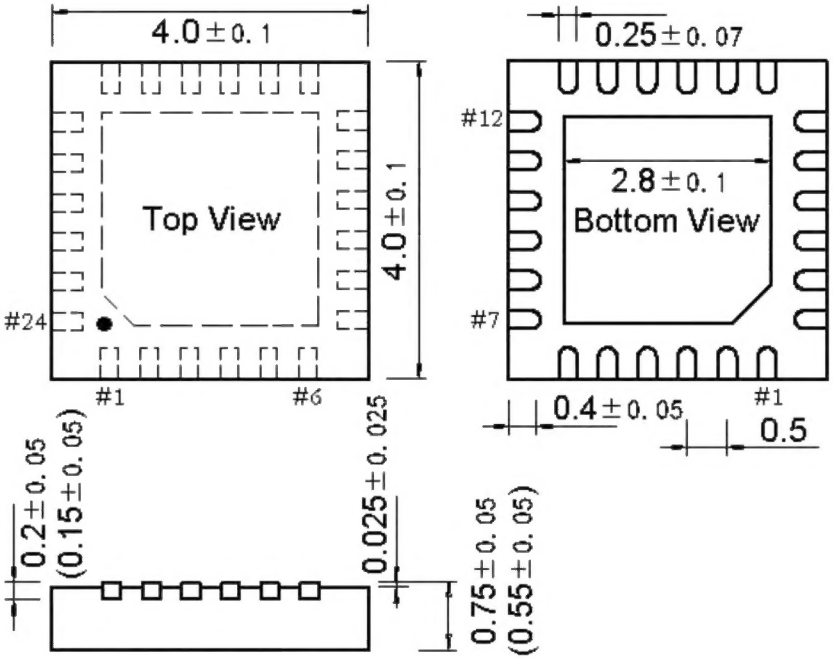
Chapter 5 Package Information

Note:

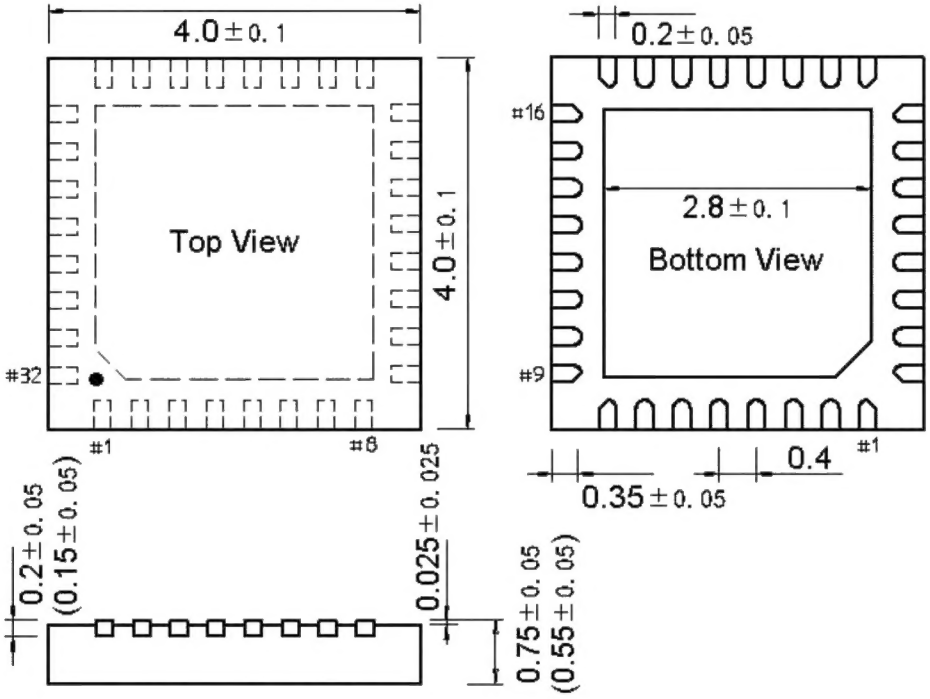
Dimensions are marked in mm (millimeters)

The pin center spacing is the nominal value without error, and the dimensional error other than that is no more than ±0.2mm.

5.1 QFN24_4x4

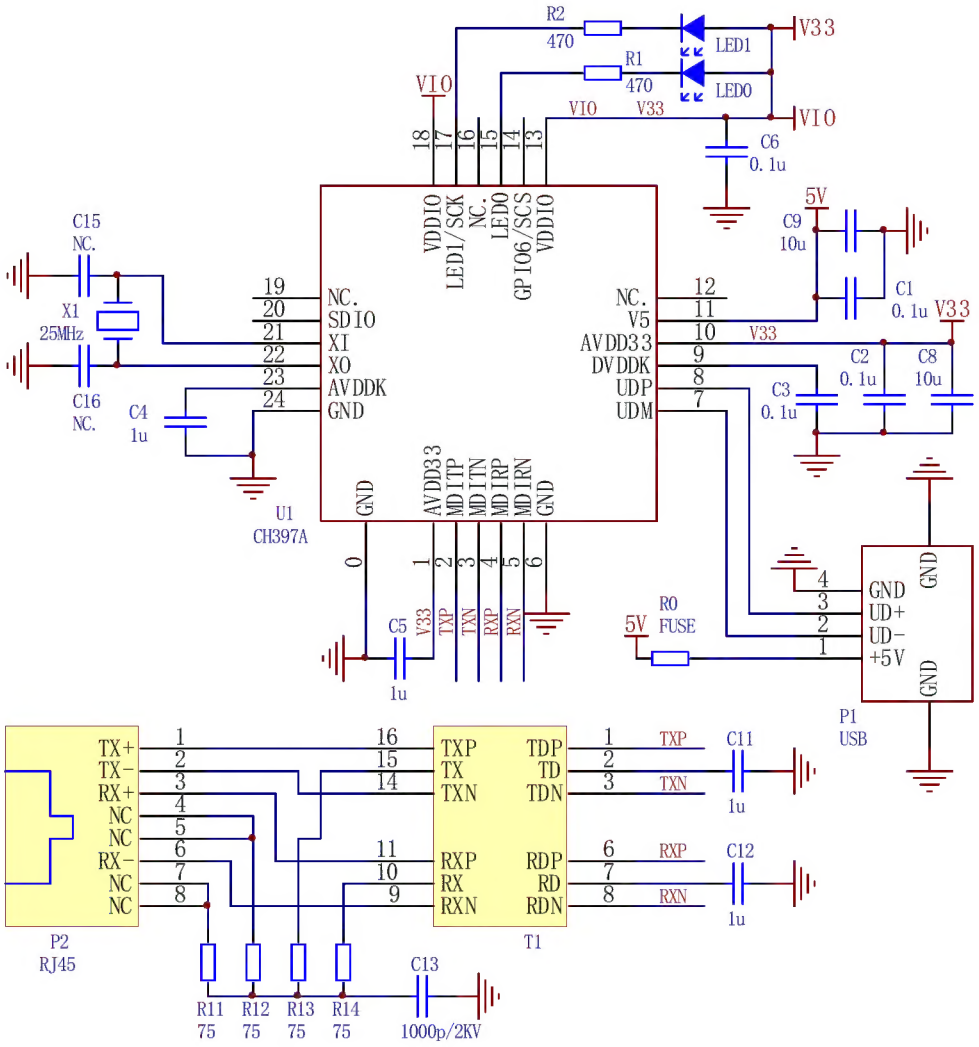


5.2 QFN32_4x4



Chapter 6 Applications

6.1 USB NIC Adapter



R1/R2/LED0/LED1 are optional LED indication. For CH397 chips with lot number penultimate 6 digit 8, the GPIO6 pin defaults to the USB configuration status indication ACT, which is active low and can be used to drive LEDs with current-limiting resistors in series.

R0 is the insurance resistor, and 0Ω resistor can be used for simplified applications. C2+C8 are two MLCC capacitors of 0.1uF and 10uF connected in parallel, a single 1uF capacitor can be used for simplified applications. C1+C9 is similar.

Industrial-grade applications are recommended to connect both V5 and AVDD33 to an external 3.3V power supply to reduce the maximum power consumption of the CH397 from 120mA*5V to 120mA*3.3V, which helps reduce the voltage drop and temperature rise of the CH397 chip.

VDDIO supports 3.3V and 2.5V, select as needed, VDDIO should be powered up and down at the same time as AVDD33, in this application directly connected to the internal LDO output of 3.3V.

If there are power supply pins with the same name, then a short connection between them should be recommended, and a short connection between several AVDD33.

CH397 has built in part of the oscillation capacitance of crystal X1, C15 and C16 can be adjusted according to the crystal parameters. For X1 with a load capacitance of 12pF, C15 and C16 are not needed; for X1 with a load capacitance of 20pF, C15 and C16 are recommended to be 15pF each.

T1 is ethernet network transformer, its center tap is grounded through capacitor C11/C12 respectively, do not connect any power supply.

CH397 has built-in Ethernet 50Ω impedance matching resistor, external do not connect 49.9Ω or 50Ω resistor, equivalent to the voltage drive.

The CH397 supports network transformer-free, capacitor-isolated Ethernet applications with slightly worse results than network transformers, refer to the application circuit diagram.

PCB design needs to consider the actual operating current carrying capacity, 5V, AVDD33 pin V33 and P1 and each port GND alignment path of the PCB as wide as possible, multiple parallel connections are recommended if there are over-holes.

It is recommended to add overvoltage protection device for 5V and ESD protection device for USB signal, such as CH412K, whose VCC should be connected to V33.

6.2 On-board USB to Ethernet

If there is an on-board 3.3V power supply, then it is recommended to connect both V5 and AVDD33 to the 3.3V power supply, and VDDIO to select the power supply according to the application.